## Experiment No.- 7

**AIM**: Understand JK Flip-Flop and implement T-Flip Flop using NAND circuit of JK Flip Flop.

**Learning Objectives:**

1. To implement JK flip flop using NAND gates and verify of its functionality.
2. To implement T flip flop using NAND gates and verify its functionality.

**Components & Instruments required:** IC 7410, 7400, Power supply and LEDs.

**Theory:**

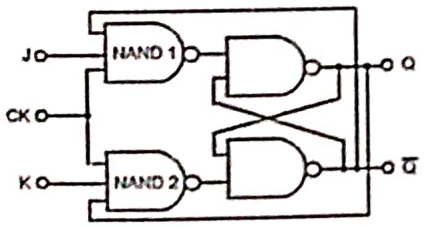
The logic circuits whose outputs at any instant of time depend not only on the present input but also on the past outputs are called sequential circuits. The simplest kind of sequential circuit which is capable of storing one bit of information is called latch. The operation of basic latch can be modified, by providing an additional control input that determines, when the state of the circuit is to be changed. The latch with additional control input is called the Flip-Flop. The additional control input is either the clock or enable input. Flip flop is formed using logic gates. Flip flop are fundamental building blocks in the memory of electronic devices. Each flip flop can store one bit of data. Based on their operations, flip flops are basically 4 types. They are

1. S-R flip flop
2. D flip flop
3. J-K flip flop
4. T flip flop

**J-K flip-flop:** JK flip flop operates on sequential logic principle, where the output is dependent not only on the current inputs but also on the previous state. There are two inputs in JK Flip Flop Set and Reset denoted by J and K. It also has two outputs: Output and complement of Output denoted by Q and $\bar{Q}$. The internal circuitry of a JK Flip Flop consists of a combination of logic gates, usually NAND gates as shown in **Figure 1.**

JK flip flop comprises four possible combinations of inputs:

- **J=0, K=0:** In this state, flip flop retains its preceding state. It neither sets nor resets itself, making it stable.
- **J=0, K=1:** This input combination forces flip flop to reset, resulting in Q=0 and $\bar{Q}$=1. It is often referred to as the "reset" state.
- **J=1, K=0:** Here, flip flop resides in the set mode, causing Q=1 and $\bar{Q}$=0. It is known as the "set" state.
- **J=1, K=1:** This combination toggles flip flop. If the previous state is Q=0, it switches to Q=1 and vice versa. This makes it valuable for frequency division and data storage applications.




| Inputs | | | Output $Q_{n+1}$ | Operation |
|---|---|---|---|---|
| CLK | J | K | | |
| 0 | X | X | $Q_n$ | No change |
| ↓ | 0 | 0 | $Q_n$ | No change |
| ↓ | 0 | 1 | 0 | Reset |
| ↓ | 1 | 0 | 1 | Set |
| ↓ | 1 | 1 | $Q_n'$ | Toggles |

**Figure 1**: J-K Flip flop using NAND gate, Truth Table (here $Q_n$=Q)

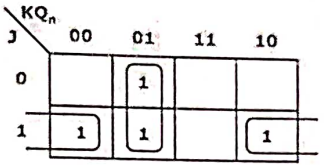
**Characteristic Table:**

| J | K | $Q_n$ | $Q_{n+1}$ | State |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | $Q_n$ (Hold) |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 0 | Reset |
| 0 | 1 | 1 | 0 | |
| 1 | 0 | 0 | 1 | Set |
| 1 | 0 | 1 | 1 | |
| 1 | 1 | 0 | 1 | Toggel |
| 1 | 1 | 1 | 0 | |

**Excitation table:**

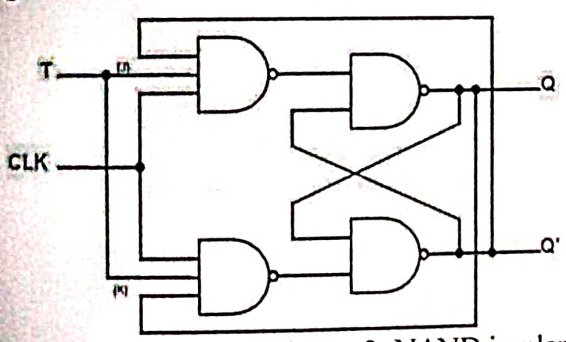
| $Q_n$ | $Q_{n+1}$ | J | K |
|---|---|---|---|
| 0 | 0 | 0 | × |
| 0 | 1 | 1 | × |
| 1 | 0 | × | 1 |
| 1 | 1 | × | 0 |

**Characteristic Equation:**




$$\Rightarrow Q_{n+1} = J\overline{Q}_n + \overline{K}Q_n$$

**T flip-flop:** T flip flop or to be precise is known as Toggle Flip Flop because it can able to toggle its output depending upon on the input. T, here stands for Toggle. Toggle basically indicates that the bit will be flipped i.e., either from 1 to 0 or from 0 to 1. The toggle or T-type flip-flop gets its name from the fact that its two outputs Q and Q invert from their previous state as it toggles back and forth every time it is triggered (T = 1). That is, the Q and Q outputs change to a "1" if it was "0", and "0" if it was previously a "1" but only when the "T" input changes HIGH, otherwise they do not change. Same is shown in Figure 2




| Clk | T | $Q_{n+1}$ | Operation |
|---|---|---|---|
| 0 | × | $Q_n$ | Memory |
| 1 | 0 | $Q_n$ | Memory |
| 1 | 1 | $Q_n$' | Toggle |

**Figure 2**: NAND implementation of T-FF and Truth Table

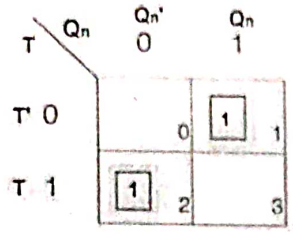
**Characteristic Table:**

| Clk | T | $Q_n$ | $Q_{n+1}$ |
|---|---|---|---|
| 0 | × | × | × |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**Excitation Table:**

| $Q_n$ | $Q_{n+1}$ | T |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

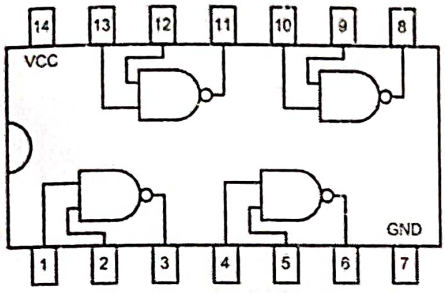
**Characteristic equation:**



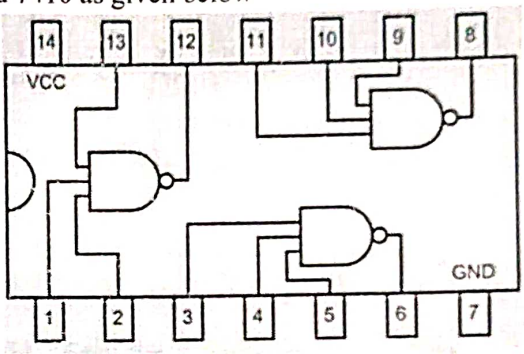

$Q_{n+1} = T\overline{Q_n} + \bar{T}Q_n = T \text{ xor } Q_n$

**Procedure:**

1. Make the connections using IC 7400 and 7410 as given below




**7400 Quad-Two input NAND**




**7410 Tripple three input NAND**

2. **Power on the IC**-7410 and 7400 by connecting $V_{CC}$ at pin 14 and GND at PIN 7.
3. Connect the "Clock 1Hz" button or pulse button as a CLK.
4. Apply the inputs as per characteristic table of JK FF and note the outputs in **Figure 1**, Update the observation table of JK FF.
5. Verify the practical and theoretical values of JK-FF as per entries in observation table of JK FF.
6. Similarly repeat step 4 and 5 for T FF of **Figure 2.**
7. Identify different sources of error in this practical.

**IC Diagram of JK-FF using NAND Gates:**

**IC Diagram of T-FF using NAND Gates**

**Precautions:**

1. Do not press the IC on breadboard until pins are aligned with pours.
2. Make connection properly.
3. There should not any short circuit in the circuit. Avoid the heating of IC. Provide proper clock pulse.

**Learning Outcomes:**

1. To learn the working of flip flops.
2. To test the IC of gates used.
3. To learn that how the present inputs and previous outputs effects present output.

**Viva Questions:**

1. What is the function of clock pulse?
2. What do you mean by race around condition?
3. How the race around condition can be removed?
4. How to convert JK to T-FF.

Worksheet of the student

**Observation Table for J-K Flip Flop**

| J | K | $Q_n$ | $Q_{n+1}$ (Calculated using Characteristic equation) | $Q_{(n+1)}$ (Observed using LED display of Digital trainer kit) |
|---|---|---|---|---|
| 0 | 0 | 0 | $J\overline{Q_n} + \bar{K}Q_n = 0.\bar{0} + \bar{0}.0 = 0.1 + 1.0 = 0 + 0 = 0$ | |
| 0 | 0 | 1 | $J\overline{Q_n} + \bar{K}Q_n = 0.\bar{1} + \bar{0}.1 = 0.0 + 1.1 = 0 + 1 = 1$ | |
| 0 | 1 | 0 | $J\overline{Q_n} + \bar{K}Q_n = 0.\bar{0} + \bar{0}.0 = 0.1 + 1.0 = 0 + 0 = 0$ | |
| 0 | 1 | 1 | $J\overline{Q_n} + \bar{K}Q_n = 0.\bar{1} + \bar{1}.1 = 0.0 + 0.1 = 0 + 0 = 0$ | |
| 1 | 0 | 0 | $J\overline{Q_n} + \bar{K}Q_n = 1.\bar{0} + \bar{0}.0 = 1.1 + 1.0 = 1 + 0 = 1$ | |
| 1 | 0 | 1 | $J\overline{Q_n} + \bar{K}Q_n = 1.\bar{1} + \bar{0}.1 = 1.0 + 1.1 = 0 + 1 = 1$ | |
| 1 | 1 | 0 | $J\overline{Q_n} + \bar{K}Q_n = 1.\bar{0} + \bar{1}.0 = 1.1 + 0.0 = 1 + 0 = 1$ | |
| 1 | 1 | 1 | $J\overline{Q_n} + \bar{K}Q_n = 1.\bar{1} + \bar{1}.1 = 1.0 + 0.1 = 0 + 0 = 0$ | |

**Observation Table for T Flip Flop**

| T | $Q_n$ | $Q_{n+1}$ (Calculated using Characteristic equation) | $Q_{(n+1)}$ (Observed using LED display of Digital trainer kit) |
|---|---|---|---|
| 0 | 0 | $T\overline{Q_n} + \bar{T}Q_n = 0.\bar{0} + \bar{0}.0 = 0.1 + 1.0 = 0 + 0 = 0$ | |
| 0 | 1 | $T\overline{Q_n} + \bar{T}Q_n = 0.\bar{1} + \bar{0}.1 = 0.0 + 1.1 = 0 + 1 = 1$ | |
| 1 | 0 | $T\overline{Q_n} + \bar{T}Q_n = 1.\bar{0} + \bar{1}.0 = 1.1 + 0.0 = 1 + 0 = 1$ | |
| 1 | 1 | $T\overline{Q_n} + \bar{T}Q_n = 1.\bar{1} + \bar{1}.1 = 1.0 + 0.1 = 0 + 0 = 0$ | |

## Practical No 8

**Aim:** Implement Decade counter using IC-7490 and seven segment display.

**Learning Objective:** To use IC-7490 as MOD-2, MOD-5 and MOD-10 counter, and display IC-7490 output value on 7 segment display through decoder circuit.

**Instruments/Components required:** IC 7490, IC 7447 Decoder, Seven Segment display, digital trainer module with 1Hz clock and 5V Power terminal, breadboard.

**Theory:** A decade counter resets to zero when the output count reaches the decimal value of 9, i.e. when 1001. A counter with a count sequence from binary 0000 through to 1001 is generally referred as a BCD binary code decimal counter because its ten state sequences ie 0,1,2,3,4,5,6,7,8,9, are Binary Coded Decimal (BCD) Numbers.

The design of the experiment requires three ICs i.e. 7490, 7447 and seven segment display. The outputs of 7490 acts as input to 7447 (BCD to seven segment decoder). There are 7 output PIN from 7447 which acts as inputs to seven segment display IC as shown in Figure 1.

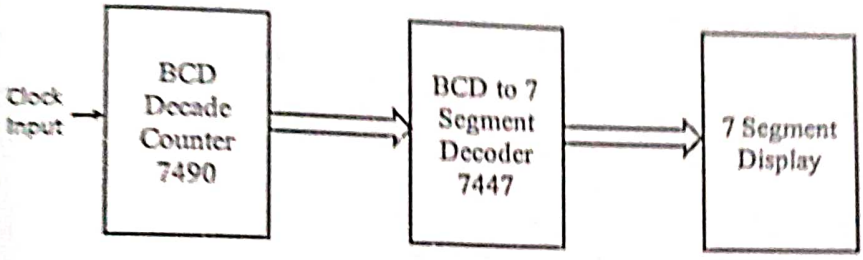



**Figure 1:** Block Diagram of the Experiment

1. **IC 7490 BCD Decade Counter:** It is a 14 pin IC, which can output the binary numbers from 0000 to 1001. After 1001 it gets resets and again starts counting from zero, as shown in **Figure 3 & 4**. Since, IC 7490 gets reset after counting ten numbers, it is called MOD-10 or Decade Counter. This IC takes 10 clock pulses to generates BCD code corresponding to each clock pulse. The outputs QA, QB, QC and QD are four bits of the BCD code.

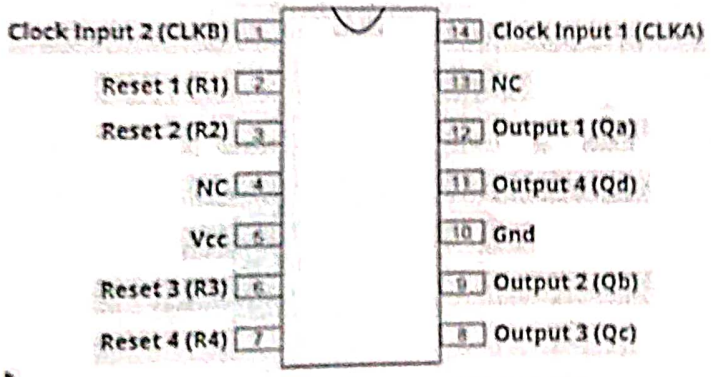



**Figure 2:** PIN diagram of IC-7490

The IC 7490 consists of MOD-2 and MOD-5 counters. MoD-2 counter has output QA and MOD-5 counter has output $Q_D$, $Q_C$ and $Q_B$ ($Q_D$ is MSB and $Q_B$ is LSB of MOD-5 counter). Count sequence of MOD-5 counter is 0→1→2→3→4→0 and so on. The count sequence of MOD-2 counter is 0→1→0 and so on. It should be noted that external CLK signal is applied at MOD-2 counter and its output $Q_A$ acts as clock for MOD-5 counter. This is shown in Figure 7. The state diagram for decade counter is as:

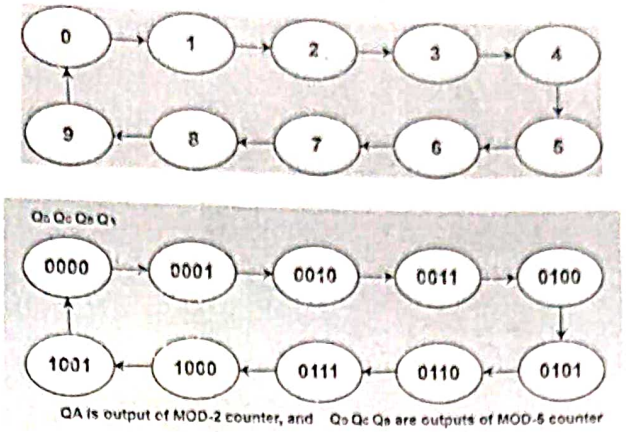



**Figure 3**: State diagram of MoD-10 Counter

| Truth table of Decade Counter | | | | | |
|---|---|---|---|---|---|
| **Clock Count** | **Output Bit Pattern for IC - 7490** | | | | **Output of decade counter in decimal value** |
| | QD | Qc | QB | QA | |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 0 | 1 | 1 |
| 3 | 0 | 0 | 1 | 0 | 2 |
| 4 | 0 | 0 | 1 | 1 | 3 |
| 5 | 0 | 1 | 0 | 0 | 4 |
| 6 | 0 | 1 | 0 | 1 | 5 |
| 7 | 0 | 1 | 1 | 0 | 6 |
| 8 | 0 | 1 | 1 | 1 | 7 |
| 9 | 1 | 0 | 0 | 0 | 8 |
| 10 | 1 | 0 | 0 | 1 | 9 |

**Figure 4:** Truth table of Decade Counter

2. **IC 7447 BCD to seven segment decoder/driver IC**: It is a 16 pin IC, which accepts a binary coded decimal as input and converts it into a pattern to drive a seven-segment for displaying digits 0 to 9. BCD is an encoding method in which each digit of a number is represented by its own binary sequence (usually of four bits). It accepts four lines of BCD (8421) input data and generates their complements internally. The outputs correspond to common anode (CA) configuration of seven segment as shown in **Figure 5**.

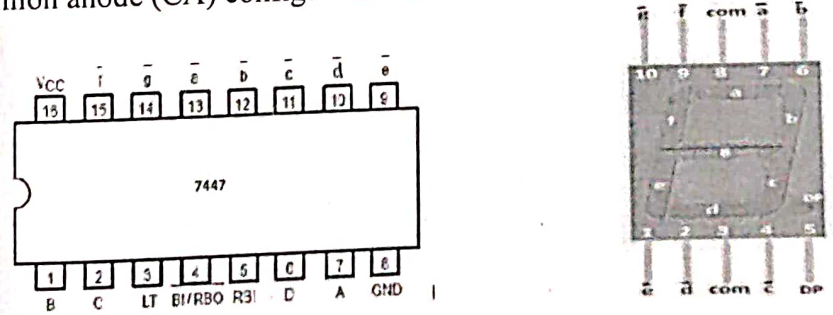


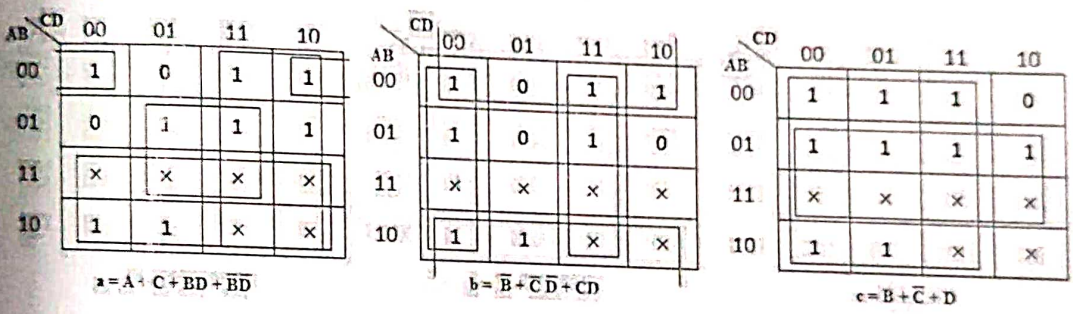

**Figure 5**: PIN diagram of IC-7447 and 7 segment display

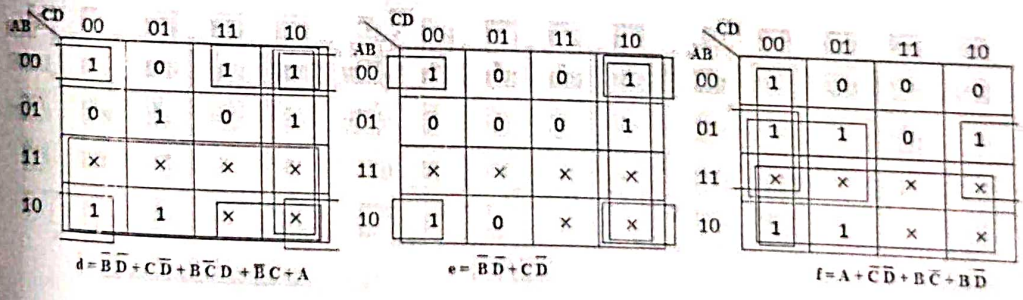
## Truth table and internal circuit of IC-7447:

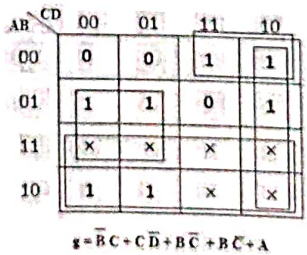
| Digit | A | B | C | D | a | b | c | d | e | f | g |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 4 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 6 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 7 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

## K-Map Simplification

The below figures show the k-map simplification for the common cathode seven-segment decoder in order to design the combinational circuit.

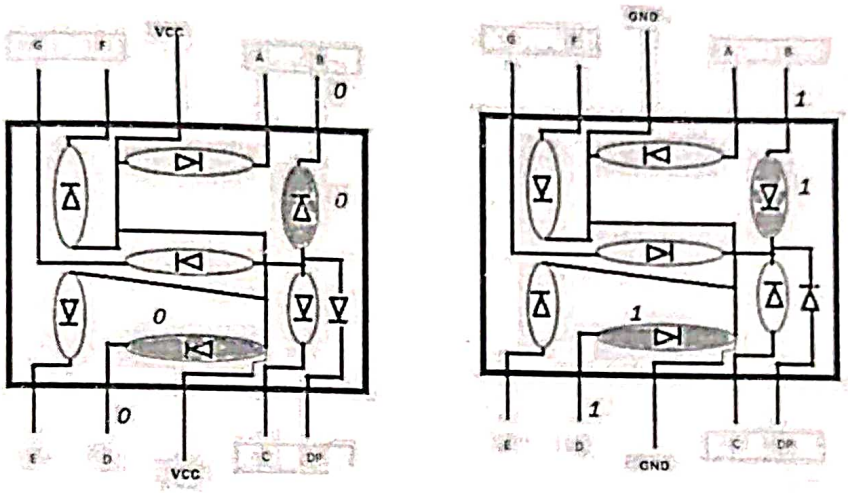


3. **Seven Segment Display:** Seven segment displays are 10 pin output display device that provides a way to display information in the form of images or text or decimal numbers, which is an alternative to the more complex dot matrix displays. It is widely used in digital clocks, basic calculators, electronic meters, and other electronic devices that displays numerical information. It consists of seven segments of light-emitting diodes (LEDs), which are assembled like numerical 8. According to the type of application, there are two types of configurations of seven-segment displays: **common anode display and common cathode display** as shown in **Figure 6.**

In common cathode seven segment displays, all the cathode connections of LED segments are connected together to logic 0 or ground. We use logic 1 through a current limiting resistor to forward bias the individual anode terminals a to g (we may also connect without using a resistance). Whereas all the anode connections of the LED segments are connected together to logic 1 in a common anode seven segment display. We use logic 0 through a current limiting resistor to the cathode of a particular segment a to g (we may also connect without using a resistance).




Common anode seven segment display (LED will glow with input LOW)

Common cathode seven segment display (LED will glow with input HIGH)

**Figure 6:** Common Anode, Common Cathode Display

## 7 Procedure:

**7.1 Power On the ICs: IC-7490:** PIN 5 to Vcc and PIN 10 to GND, **IC-7447:** PIN 15 to Vcc and PIN 8, **7-Segment display:** PIN 8 and or 3 to Vcc through a resistance to provide less than 5V to power on display IC.

**7.2 Connection diagram: -** The output of IC-7490 is connected to IC7447 decoder and decoder output to 7-segment display unit. Make the connections as shown in **Figure 7,** as per case-2 of observation table.

**7.3 Case-1 of Observation table:**

7.3.1 Master CLK of 1Hz taken from Trainer module is connected at PIN -14 of IC-7490.

7.3.2 PIN-12 is not connected to PIN-1 of IC-7490

**7.4 Case-2 of Observation table:**

7.4.1 Master CLK of 1Hz taken from Trainer module is connected at PIN -14 of IC-7490.

7.4.2 PIN-12 is connected to PIN-1 of IC-7490.

**7.5 Case-3 of Observation table:**

7.5.1 Master CLK of 1Hz taken from Trainer module is not connected at PIN -14 of IC-7490.

7.5.2 PIN-12 is not connected to PIN-1 of IC-7490

7.5.3 Master CLK of 1Hz taken from Trainer module is connected at PIN -1 of IC-7490

**Observation Table**

| Sr No | Changes in connection diagram of Figure 7 | Expected sequence | Observed Sequence |
|---|---|---|---|
| Case: 1 | 1) Master CLK of 1Hz taken from Trainer module is connected at PIN -14 of IC-7490 and<br>2) PIN-12 is not connected to PIN-1 of IC-7490 | 0→ 1→0 | |
| Case: 2 | 1) Master CLK of 1Hz taken from Trainer module is connected at PIN -14 of IC-7490 and<br>2) PIN-12 is connected to PIN-1 of IC-7490 | 0→1→2→3→4 →5→6→7→8 →9→0 | |
| Case: 3 | 1) Master CLK of 1Hz taken from Trainer module is not connected at PIN -14 of IC-7490 and<br>2) PIN-12 is not connected to PIN-1 of IC-7490<br>3) Master CLK of 1Hz taken from Trainer module is connected at PIN -1 of IC-7490 | 0→1→2→3→4 →0 | |

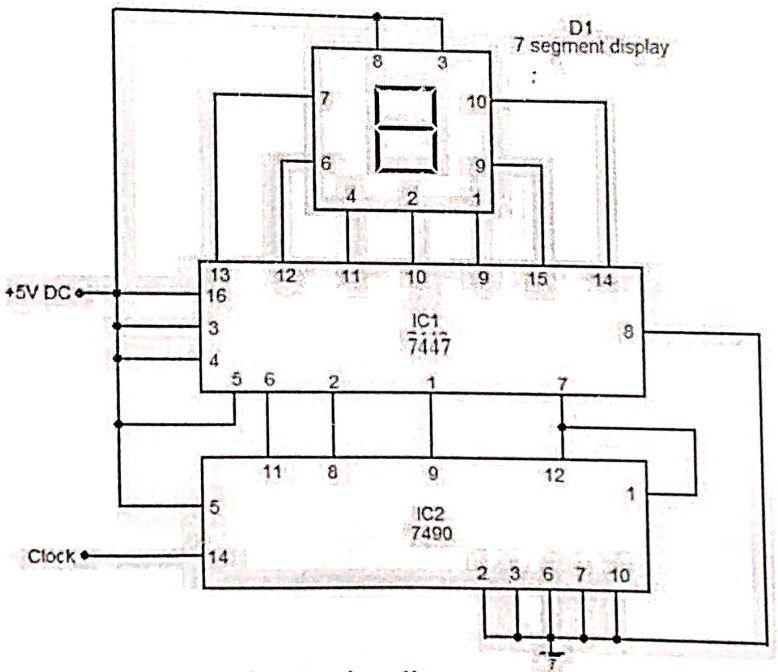



**Figure 7**: Connection diagram as per CASE-2

**8 Precautions:**

8.1 Do not press the IC on breadboard until pins are aligned with pours.

8.2 Make connection properly.

8.3 There should not any short circuit in the circuit.

8.4 Avoid the heating of IC.

8.5 Provide proper clock pulse.

## 9 Viva Questions:

9.1 Which type of seven segment display IC is used in this experiment?
9.2 What should be the value of a, b, c, d, e, f and g, if we have to display 6?
9.3 What do you understand by MOD-10 counter?

## 10. Learning Outcomes (expected):

10.1 Connect the circuit diagram using breadboard, and Digital Trainer module.
10.2 Use IC7490 as MoD-2. MoD-5 and MoD-10 Counter.
10.3 Identify Common anode and common cathode display.
10.4 Identify faults in the connection diagram.

## 11. Learning Outcomes (What I have learnt):

## IC Connection Diagram: